

Vishay Siliconix

Dual N-Channel 150-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

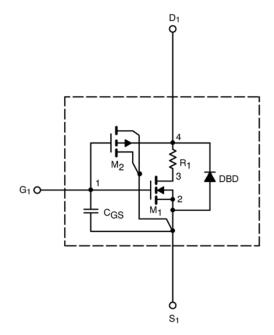
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

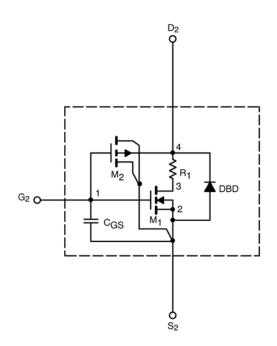
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UN	NLESS OTHERV	VISE NOTED)			
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V_{DS} = V_{GS} , I_D = 250 μ A	2.6		V
On-State Drain Current ^a	I _{D(on)}	$V_{\text{DS}}~\geq 5$ V, V_{GS} = 10 V	39		А
Drain-Source On-State Resistance ^a	r _{DS(on)}	V_{GS} = 10 V, I _D = 3.3 A	0.123	0.124	Ω
		V _{GS} = 6 V, I _D = 3.1 A	0.133	0.137	
Forward Transconductance ^a	g _{fs}	V_{DS} = 15 V, I_{D} = 3.3 A	6	9	S
Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = 2.9 A, $V_{\rm GS}$ = 0 V	0.83	0.87	V
Dynamic ^b					
Total Gate Charge	Qg	V_{DS} = 75 V, V_{GS} = 10 V, I_{D} = 3.3 A	12	12.6	nC
Gate-Source Charge	Q _{gs}		2.8	2.8	
Gate-Drain Charge	Q _{gd}		4.5	4.5	
Turn-On Delay Time	t _{d(on)}	V_{DD} = 75 V, R _L = 75 Ω I _D \cong 1 A, V _{GEN} = 10 V, R _G = 6 Ω	13	11	ns
Rise Time	tr		13	15	
Turn-Off Delay Time	t _{d(off)}		32	30	
Fall Time	t _f		14	20	

Notes a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si7946DP

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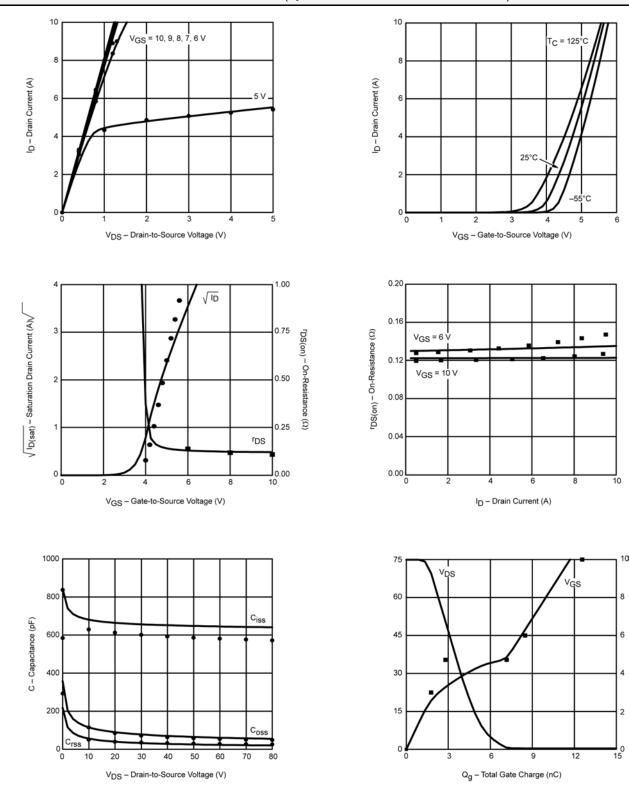
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COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data



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